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For

FULLY DIFFERENTIAL AMPLIFIER WITH START UP CIRCUIT

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FULLY DIFFERENTIAL AMPLIFIER WITH START UP CIRCUIT

FIELD

[0001] Embodiments of this invention relate to the field of circuits and, in particular, to amplifier circuits.

BACKGROUND

[0002] In the design of complementary metal-oxide semiconductor (CMOS) integrated circuits, differential amplifiers are used for various applications because a number of advantages can be derived from these types of amplifiers, as compared to single-ended amplifiers. Differential amplifiers are used to amplify analog, as well as digital signals, and can be used in various implementations to provide an output from the amplifier in response to differential inputs. For example, a general-purpose differential amplifier amplifies the difference of the two input signals. But these differential amplifiers can be readily adapted to function as an operational amplifier, a comparator, a sense amplifier and as a front-end buffer stage for another circuit, etc. Differential amplifiers are utilized where linear amplification having a minimum of distortion is desired. A fully differential amplifier differs from a differential amplifier in that its outputs are also differential. Using a fully differential design gives a designer a way to dramatically reduce the common mode noise present in the system and the second harmonic in the fast fourier transform of the output signal.

[0003] Figure 1A illustrates a conventional fully differential amplifier. The fully differential amplifier shown in Figure 1A is a two-stage amplifier with a common mode feedback CMFB controlling the first stage, load transistors M3 and M4. A common mode feedback input CMIN signal is supplied by the resistor/capacitor chain: R1, R2, C1,

and C2. In some applications such as switch capacitor networks, there can be a state where the amplifier inputs are connected with its outputs, as illustrated in Figure 1B. If for some reason there is positive supply (VCC) voltage on both outputs VOUTP & VOUTN, a common mode feedback amplifier AMPCM will be saturated, both load and input transistors M1-M2 of the main amplifier are in a cut off state, and the nodes n1, n2 are in an undefined condition. Under this condition, any small leakage to ground on these nodes will cause the state to be stable and the amplifier may never get out of this state. As such, the amplifier will be in a stable, but undesired state of operation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Embodiments of the present invention are illustrated by way of example and not intended to be limited by the figures of the accompanying drawings.

[0005] Figure 1A illustrates a conventional fully differential amplifier.

[0006] Figure 1B illustrates a conventional fully differential amplifier having its inputs connected to its outputs.

[0007] Figure 2 illustrates one embodiment of a fully differential amplifier having a start-up circuit.

[0008] Figure 3 illustrates one embodiment of the fully differential amplifier of Figure 2 having its inputs connected to its outputs.

[0009] Figure 4 illustrates another embodiment of a fully differential amplifier having an alternative start-up circuit.

[0010] Figure 5 illustrates one embodiment of external component connections to the fully differential amplifier.

[0011] Figure 6 illustrates a system including an embodiment of the fully differential amplifier.

[0012] Figure 7 illustrates an alternative embodiment of a common mode feedback network.

DETAILED DESCRIPTION

[0013] In the following description, numerous specific details are set forth such as examples of specific systems, circuits, components, etc. in order to provide a thorough understanding of embodiments of the present invention. It will be apparent, however, to one skilled in the art that these specific details need not be employed to practice embodiments of the present invention. In other instances, well known components or methods have not been described in detail in order to avoid unnecessarily obscuring embodiments of the present invention.

[0014] A fully differential amplifier having a start-up circuit is described. In one embodiment, the fully differential amplifier may be a two-stage amplifier with a start-up circuit coupled between the stages. In one embodiment, the start-up circuit may include a sense circuit coupled between a common mode input and internal nodes that are connect to output transistors of the fully differential amplifier.

[0015] The apparatus and methods discussed herein provide a solution to an issue where the fully differential amplifier might turn on at an undesired stable working point, at which the amplifier will not function at all. In such a case, the apparatus and methods described herein may automatically produce a reset signal at the output of the sense circuit that will lower the outputs of the fully differential amplifier and place it in a normal operation mode.

[0016] Figure 2 illustrates one embodiment of a fully differential amplifier having a start-up circuit. In this embodiment, amplifier 200 includes a start-up circuit coupled to core amplifier circuitry. The start-up circuit may include sense circuit 250 and pull up circuit 240. In one embodiment, the core amplifier circuitry may be a two-stage amplifier

with the first stage composed of a common mode feedback (CMFB) amplifier 260 and a second stage 261 having input transistors 301, 302 and output gain transistors 311, 312. Transistors 315, 313, 316, 305, 317, 314, 310, 320 and 321 form the bias, loads (current mirrors) for the first and second stages and the start-up circuit. The bias and current mirror (load) transistors may be considered as devices within or external to the first and second stages and the start-up circuit. In alternative embodiments, amplifier 200 may have more than two stages.

[0017] In one embodiment, the first stage CMFB amplifier 260 includes input transistors 306 and 307 coupled to load transistors 308 and 309, respectively. Input transistor 306 has a gate coupled to receive a common (COM) signal. The drain and gate of load transistor 309 of first stage CMFB are coupled to controls of the first stage 261 load transistors 303 and 304 via CMFB 269.

[0018] In one embodiment, a common mode feedback input CMIN 259 signal may be generated using a common mode resistor/capacitor (RC) feedback network 262. The CMIN 259 signal of common mode RC feedback network 262 closes the common mode feedback loop amplifier's main outputs OUTP 211 and OUTN 212 via the AMPCM amplifier input of transistor 307 and load transistors 303 and 304. The resistors R1 and R2 provide the function (OUTP-OUTN)/2, thus extracting a common mode signal. The capacitors C1 and C2 do the same function (OUTP-OUTN)/2 for high frequencies. In another embodiment, CMIN 259 signal may be generated by a switching capacitor network 762 as illustrated in Figure 7. Switching capacitor network 762 includes capacitors C1, C2, C3 and C4 and switches 711-716. The operation of a switching capacitor network is known in the art; accordingly, a detailed discussion is not

provided. Alternatively, the CMIN 259 signal may be generated using other circuit configurations known in the art.

[0019] A sense circuit 250 is coupled between the first stage AMPCM 260 and the second stage 261. In one embodiment, the sense circuit 250 may be an amplifier having transistors 322 and 323. Transistor 323 is part of a current mirror that establishes a predefined small current through transistor 322. The gate of transistor 322 is coupled to the common mode feedback input CMIN 259 signal. In one embodiment, CMIN 259 signal may be configured to be approximately less than half VCC 209 (e.g., in one embodiment about 1V) that turns on transistor 322 and, thereby, shorts the sense circuit output 255 to VCC. Sense circuit output 255 is coupled to the gates of transistors 318 and 319. The shorting of sense circuit output 255 to VCC 209 generates a reset signal that closes transistors 318 and 319 such that no currents are inserted into node (n1) 221 and node (n2) 222. When the potential on both outputs OUTP 211 and OUTN 212 goes to VCC 209 and turns off transistor 322, the sense circuit output 255 goes low and the current from VCC 209 begins to charge nodes 221 and 222. The charge on nodes 221 and 222 is large enough to cause the voltage on these nodes to rise and turn on transistors 311 and 312, which in turn, lowers the outputs OUTP 211 and OUTN 212, thereby causing the main CMFB 269 to operate and close the sense circuit 250 and transistors 318 and 319.

[0020] Figure 3 illustrates one embodiment of the fully differential amplifier of Figure 2 having its inputs connected to its outputs. In some applications where amplifier 200 may be used (e.g., a switch capacitor network), there can be a state where the amplifier 200 has its inputs 201 and 202 connected with its outputs 211 and 212,

respectively, via switch (SW) 331 and switch 332. If there is positive supply voltage VCC 209 on both outputs OUTP 211 and OUTN 212, the common mode feedback amplifier (AMPCM) 260 of Figure 2 will be saturated (turned off). When the common mode feedback amplifier 260 is saturated, the input transistors 301 and 302 and the load transistors 303 and 304 are in a cut off state, and the nodes 221 and 222 may otherwise be in an undefined condition without sense circuit 250. Sense circuit 250 may operate to avoid a possible state where the amplifier's state is stable but in an undesired state of operation.

[0021] Sense circuit 250 may enable a normal mode of operation for amplifier 200 under various starting condition and, thereby, eliminate the possibility of amplifier 200 getting into a non-operating state under various sequences of turn-on or turn-off of voltage supplies VCC 209 and signals input and output on INP 201, INN 202 and OUTP 211, OUTN 212, respectively. A non-operating state can happen when the input transistors 301 and 302 are turned off (e.g., the input voltage is near VCC). When this happens, the potential at nodes 221 and 222 is undefined and can be very low near ground. Transistors 311 and 312 are also turned off and the outputs OUTP 211 and OUTN 212, respectively, go high to VCC 209. One cause of such a state may be the connection shown in Figure 3.

[0022] Referring again to the embodiment of Figure 2, transistors 319, 318 and sense circuit 250 form the start-up circuit. Transistor 319 is coupled (via bias transistor 317) between VCC 209 and node 221 and transistor 318 is coupled (via current source transistor 316) between VCC 209 and node 222, respectively, and form a pull-up circuit 240. The pull-up circuit 240 operates to bring nodes 221 and 222 to a high potential

value high enough to turn on transistors 311 and 312. As previously discussed, the turning on of transistors 311 and 312 lowers the outputs OUTP 211 and OUTN 212 and returns amplifier 200 to its normal operation mode. The normal operation mode of amplifier 200 is when the amplifier is functional to amplify an input differential signal at INP 201, INN 202. In the normal operation mode, the input transistors 301 and 302 are not turned off (have current flowing through them) and the common mode of the outputs is maintain near the COM 268 signal value (with common mode loop error). In one exemplary embodiment, the COM 268 signal value may be approximately in a range of 1 volt to VCC/2 volts. Alternatively, COM 268 signal values outside the provided exemplary range may be used. The start-up circuit of fully differential amplifier 200 may have other configurations, for example, as discussed below in relation to Figure 4.

[0023] Figure 4 illustrates another embodiment of a fully differential amplifier 200 having an alternative start-up circuit 450. In this embodiment, start-up circuit 450 includes current source transistors 316 and 317. When the amplifier 200 is in a non-operational mode, the constant currents from transistors 316 and 317 charge nodes 222 and 221, respectively, and turn on transistors 311 and 312, respectively. These constant currents that exist even in the normal operational mode insert an additional error on the common mode value in this embodiment that, if great enough, add to the current consumption of the circuit. One way to address this error is to turn off these currents in the normal operation mode by means of a sense circuit and switches, for example, as illustrated in the embodiment of figure 2.

[0024] Figure 5 illustrates one embodiment of external component connections to fully differential amplifier 200. Fully differential amplifier 200 may be used to amplify

analog, as well as digital signals, and can be used in various implementations to provide an output from the amplifier in response to differential inputs. The fully differential amplifier 200 amplifies the difference of the two input signals that can be readily configured to operate as a variety of circuits, for example, an analog to digital converter (ADC), an automatic gain control (AGC) amplifier, a filter, a multiplexer, etc. Fully differential amplifier 200 may have one or more external components (C) 501-504 coupled to the inputs 201, 202 and/or outputs 211, 212 in order to configure fully differential amplifier 200 to operate as a particular amplifier circuit 500 (e.g., ADC, AGC, filter, multiplexer, etc). Each of the external components 501-504 may include one or more passive devices (e.g., resistor, capacitor) or active devices (e.g., transistor) or no devices (e.g., a shorted connection). The configuration of a differential amplifier into amplifier circuit 500 is known in the art; accordingly a detailed discussion is not provided.

[0025] Figure 6 illustrates a system including an embodiment of a fully differential amplifier. In this embodiment, fully differential amplifier 200 may be used in one or more circuit blocks of a wireless network interface card (NIC) 600. In this embodiment, wireless NIC 600 may include an antenna 610, RF circuitry 611 (e.g., composed of low noise amplifiers, RF AGCs, up/down frequency converters, frequency synthesizer, etc.), a base band receiver (Rx)/transmitter (Tx) 615 to wirelessly receive and transmit receive analog (e.g., radio frequency) signals, a converter 660 to covert between analog and digital signals, and a digital signal processor 650 to process the digital signals. Converter 660 may include an ADC 630 to convert received analog signals to digital signals and a DAC to convert digital signals to analog signal for

transmission by Tx 615 to antenna 610. In another embodiment, another type of processor may be used instead of DSP 650, for example, a general purpose processor. In an alternative embodiment, the blocks shown in Figure 6 may reside on one or more other carrier substrates (e.g., motherboard, daughter card, etc.).

[0026] One or more of the blocks of wireless NIC 600 (e.g., base band filter 620, ADC 630, DAC 640) may include one or more of fully differential amplifier 500 of figure 5. For example, in one embodiment, the base band receiver 620 may include one or more of fully differential amplifier 500 configured as an AGC and a filter for gain control and noise filtering of analog signals received from antenna 610. In one embodiment, base band transmitter 625 may include a fully differential amplifier 500 configured as a filter for noise filtering of analog signals output from DAC 640. In one embodiment, antenna 610 may be a dipole antenna for short to medium wave radio frequency broadcasting. Alternatively, other types of antenna may be used.

[0027] It should be noted that one or more of the transistors of the fully differential amplifier 200 discussed herein may be viewed as current sources and sinks, so that other devices or circuits having these functions may be employed. Embodiments of the present have been illustrated with Complementary Metal Oxide Semiconductor (CMOS) technology for ease of discussion. In alternative embodiments, other device types and process technologies may be used, for example, Bipolar, NMOS, PMOS, and BiCMOS. VCC is used to represent a voltage supply utilized by the circuit illustrated herein. It should be noted that the circuits described herein may be designed utilizing various voltage supplies.

[0028] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.